

# GENIO IC/Package Co-Design EDA Tool First to Offer End-to-End Optimization



By AIT News Desk

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OPTIMIZATION NEWS

MZ Technologies underscored several key IC/package co-design features that are critical to meeting today's high-performance [advanced technology](#) IC device needs. The company's GENIO IC/Package Co-Design EDA tool is the industry's only end-to-end optimized solution that covers all the requirements.

Visionary IC systems designers have identified seven key features that should be incorporated into the ideal integrated IC/package co-design tool. These include: IC, package PCB design environment support, system-level I/O planning and [optimization](#), a holistic design environment, mixed silicon and photonics, interconnect optimization, open standards, and tool agnostic work flows.

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GENIO is the only EDA tool that provides all seven, integrating silicon and package EDA flows to create a full co-design and end-to-end optimized design environment for complex multi-chip designs that comprise advanced heterogeneous microelectronic systems.

"The IC/Packaging co-design tool segment today is swiftly maturing, but none of the Big 3 have yet to offer an optimized end-to-end solution. Because we imagined and built the technology platform from the ground up, GENIO is architected from a 'design first' rather than a 'proprietary technology first' perspective," explained Anna Fontanelli, Founder and CEO of MZ Technologies.

GENIO's holistic design environment dramatically shortens design cycle time through unique features that include cross-hierarchical, 3D-aware, design methodologies that streamline the entire IC eco-system. It has proven to be very

application and packaging friendly, featuring quick IC, package, system constraints definition/import/export and a seamless interface with existing EDA environment and custom design flows.

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The result is right-the-first-time concept-to-design methodology, thanks to strong “what-if” analysis and system level exploration across architectures. GENIO identifies the most proficient solution and avoids entering “dead-end” architectures/design roads. At the same time, it automates and optimize hundreds of thousands of connections, minimizing the number of physical resources needed for system interconnect.

GENIO also eliminates design environment boundaries to enable system architectural exploration that identifies errors and bottleneck early in the design process. It also features cross-hierarchical pathfinding for pin assignment optimization, wire lengths/crossovers reduction, and floor planning-aware silicon interposer design.

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