Panel Session: Will 3D-IC Remain a Technology of the Future... Even in the Future?

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# Of Package Pins Quasi-Flat

Bandwidth AND Performance Limited by I/O Resources

Lack of Package-Interposer-Die Co-Design Critical

- Moore’s Law applies to transistors, not speed
  - Transistor count keeps doubling every 2 years
  - Transistor speed is bound by power
- Number of I/O pins per package basically flat
  - Limited by die area and/or package technology
  - Only improvement is increased I/O speed
- Bandwidth ultimately limited by I/O
  - Throughput per chip = # I/O pins * I/O speed
  - No matter how many transistors are on-chip

Source: A. Bechtolsheim, Arista Networks, 2012
Package-Interposer-Die Co-Design

I/O Planning and Optimization Technology, Integrated with Package and IC Design Tools via Standard Formats
Package-Interposer-Die Co-Design

Limited Proprietary Solutions, None Commercial

• Lack of expertise
  – Unavailable in EDA companies
  – Requires investments to be acquired/developed

• One solution doesn’t fit everybody’s needs
  – Customers have different requirements
  – Collaboration is critical

• TAM/ROI too small for leading EDA companies
  – Package design TAM is tiny
...My 2 Cents: 2.5D- And 5.5D-IC

Horizontal Connections Much Cheaper than Vertical Ones

TSV Pitch $\sim 40\mu$ vs. M10 $\sim 0.8\mu$ (at 28 Nanometers)
Thanks!

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