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Create, Innovate, Realize

Panel Session: Will 3D-IC Remain a Technology of the Future… Even in the Future?

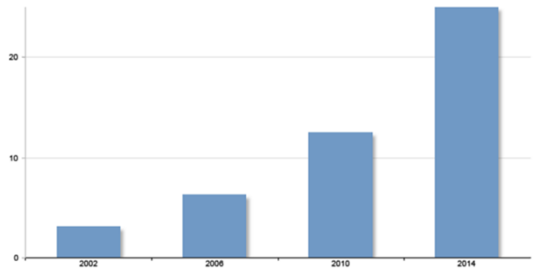
Anna Fontanelli
Founder & CEO

Of Package Pins Quasi-Flat

Bandwidth AND Performance Limited by I/O Resources
Lack of Package-Interposer-Die Co-Design Critical

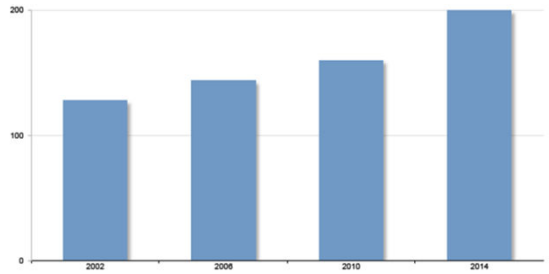
SERDES Speed (high-density CMOS)

Gbps



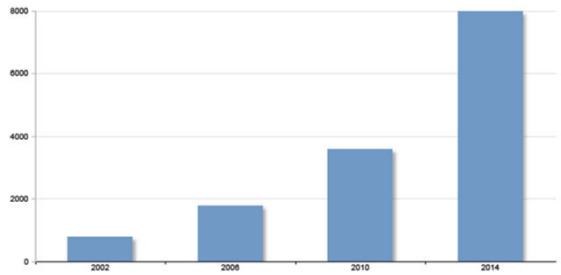
Number of SERDES per Package

# of SERDES



Maximum Throughput per Chip

Gbps



- **Moore's Law applies to transistors, not speed**
  Transistor count keeps doubling every 2 years
  Transistor speed is bound by power
- **Number of I/O pins per package basically flat**
  Limited by die area and/or package technology
  Only improvement is increased I/O speed
- **Bandwidth ultimately limited by I/O**
  Throughput per chip = # I/O pins * I/O speed
  No matter how many transistors are on-chip

Source: A. Bechtolsheim, Arista Networks, 2012

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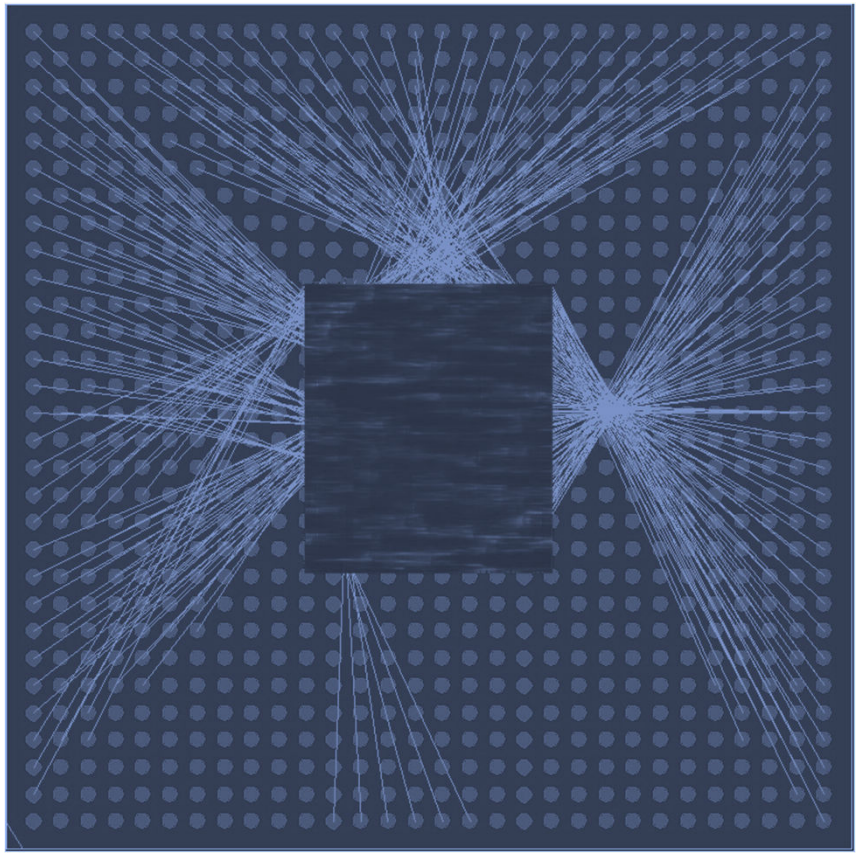
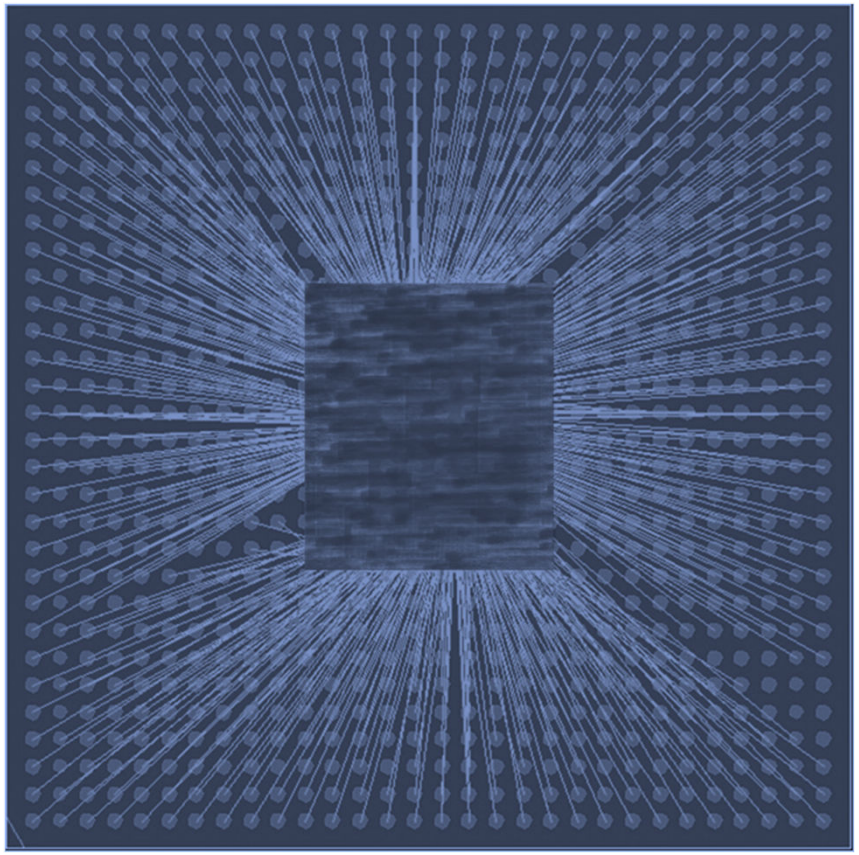
Package-Interposer-Die Co-Design

I/O Planning and Optimization Technology, Integrated with Package and IC Design Tools via Standard Formats





Package-Interposer-Die Co-Design

Limited Proprietary Solutions, None Commercial

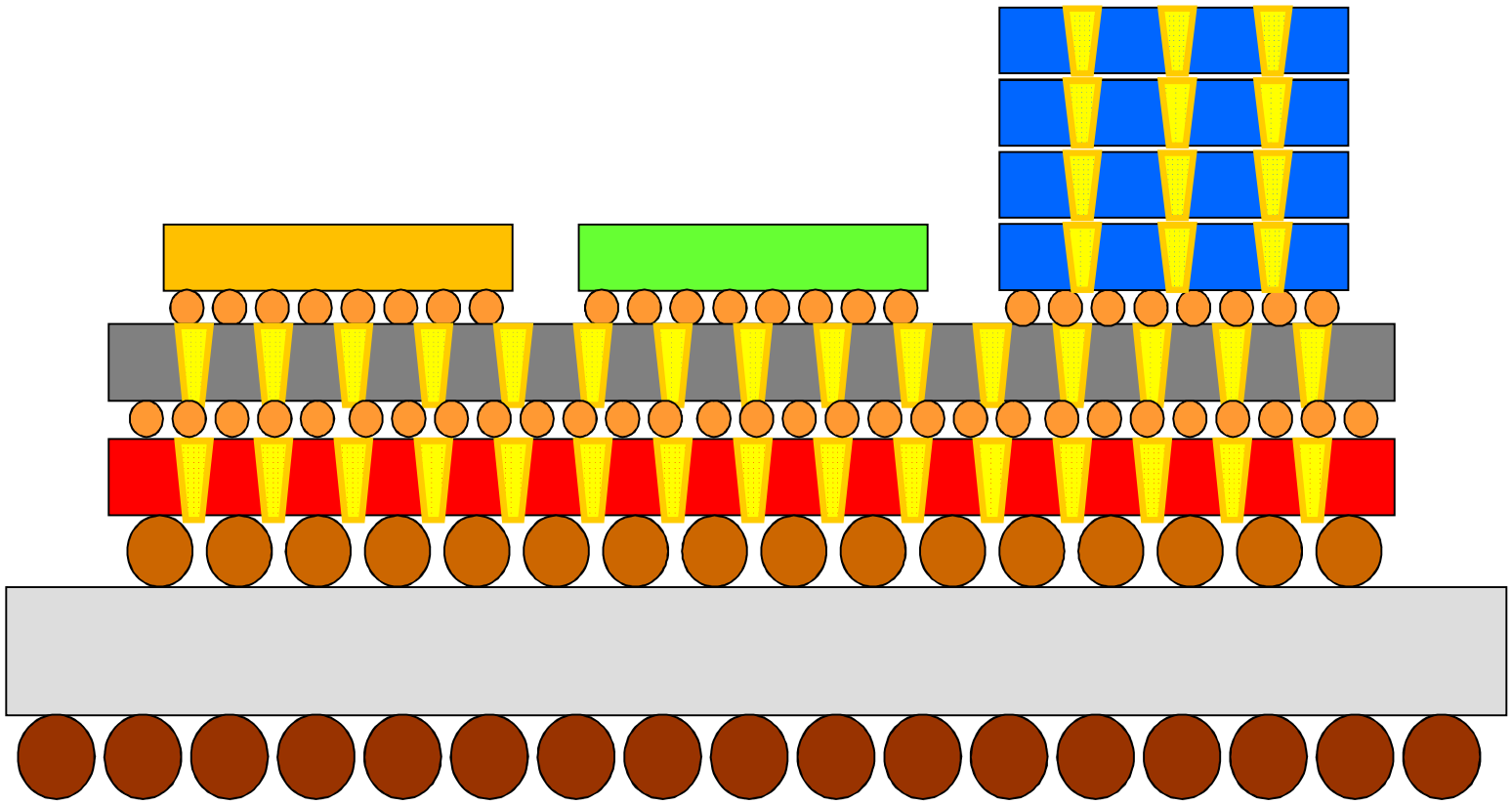
- Lack of expertise
  - Unavailable in EDA companies
  - Requires investments to be acquired/developed
- One solution doesn't fit everybody's needs
  - Customers have different requirements
  - Collaboration is critical
- TAM/ROI too small for leading EDA companies
  - Package design TAM is tiny

Source: EDAC Market Statistics, 2012

…My 2 Cents: 2.5D- And 5.5D-IC

Horizontal Connections Much Cheaper than Vertical Ones

TSV Pitch ~ 40μ vs. M10 ~ 0.8 μ (at 28 Nanometers)



Thanks !

Grenoble, France

March 21st, 2013